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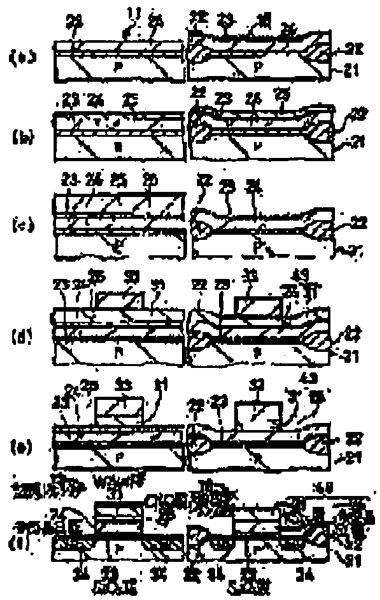
## (54) LAMINATED-GATE TYPE NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

(57)Abstract:
PURPOSE: To increase reliability and achieve high integration by reducing difference in level and to reduce a manufacturing cost by simplifying a manufacturing process and to achieve further high integration by reducing the area of a memory cell.
CONSTITUTION: A floating gate electrode and a control gate electrode in a memory transistor 13 are respectively constituted of a conducting film of of the same layer as a polycrystalline Si film 24 and a WSix film 31 constituting a control gate electrode in a peripheral-circuit transistor 19. For this reason, as compared with the constitution in which a control gate electrode or the like is formed of the polycrystalline Si film 24 and the WSix film 31, the difference in level of a memory transistor 13 is smaller and it is easier to make flat and the manufacturing process is simpler.



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## CLAIMS

[Claim(s)]
[Claim 1] The 1st insulated-gate field-effect transistor by which the floating-gate electrode is prepared through the 1st insulator layer on the channel field, and the laminating of the 1st control gate electrode is carried out through the 2nd insulator layer on this floating-gate electrode, In the laminating gate mold non-volatile semiconductor memory which has the 2nd insulated-gate field-effect transistor by which the 2nd control gate electrode is prepared on the channel field through the 3rd insulator layer of the same layer as said 1st insulator layer The laminating gate mold non-volatile semiconductor memory characterized by constituting said 2nd control gate electrode by the 1st electric conduction film of the same layer as said floating-gate electrode, and the 2nd electric conduction film by which the laminating is carried out on said 1st electric conduction film in the same layer as said 1st control gate electrode.
[Claim 2] The laminating gate mold non-volatile semiconductor memory according to claim 1 characterized by said 1st control gate electrode consisting of the semi-conductor film.
[Claim 3] The laminating gate mold non-volatile semiconductor memory according to claim 1 characterized by said 1st control gate electrode consisting of the silicide film.
[Claim 4] The laminating gate mold non-volatile semiconductor memory according to claim 2 or 3 characterized by preparing the semi-conductor nitride in the pair plane of composition with said 1st control gate electrode among said 2nd insulator layer.

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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the laminating gate mold non-volatile semiconductor memory which has the 1st insulated-gate field-effect transistor which has the floating-gate electrode, and the 2nd insulated-gate field-effect transistor which does not have the floating-gate electrode.
[0002]
[Description of the Prior Art] Drawing 4 shows the memory sections 11, such as EPROM of a NOR mold, and a flash EEPROM. In these NOR mold non-volatile semiconductor memories, the field insulator layer 12 is selectively formed in the front face of a semi-conductor substrate, the component isolation region is divided and gate dielectric film (not shown) is formed in the front face of the component active region surrounded by the field insulator layer 12.
[0003] On the channel field of the storage transistor 13 corresponding to a memory cell, the floating-gate electrode 14 is formed through gate dielectric film, and the laminating of the control gate electrode 15 is carried out through the insulator layer for capacity coupling (not shown) on this floating-gate electrode 14. The diffusion layer 16 as the source and the drain of the storage transistor 13 is formed in the component active region of the both sides of the floating-gate electrode 14 and the control gate electrode 15.
[0004] The control gate electrode 15 grade is covered with the interlayer insulation film (not shown), and the contact hole 17 which reaches the diffusion layer 16 as a drain is punctured by the interlayer insulation film etc. And the bit line (not shown) is in contact with the diffusion layer 16 as a drain through this contact hole 17.
[0005] Drawing 5 shows the approach for manufacturing the 1st conventional example of this invention which is the NOR mold non-volatile semiconductor memory shown in drawing 4 about the storage transistor 13 of the memory section 11, and the circumference circuit transistor 19 of the circumference circuit section 18. As shown in drawing 5 (a) by this manufacture approach, it is SiO2 as a field insulator layer 12 to the front face of the Si substrate 21 of P type. The film 22 is selectively formed by the LOCOS method, a component isolation region is divided, and it is SiO2. It is SiO2 as gate dielectric film to the front face of the component active region surrounded by the film 22. The film 23 is formed.
[0006] Then, the polycrystal Si film 24 is made to deposit on the whole surface with a CVD method, and it is POCl3. Lynn is added on the polycrystal Si film 24 by the pre deposition method to which it puts to a steam and thermal diffusion of Lynn is carried out from this steam. And it leaves the polycrystal Si film 24 of the shape of stripes which extends in the direction vertical to the extension direction of the control gate electrode 14 formed behind at RIE to the polycrystal Si film 24 only to the memory section 11.
[0007] Next, as are shown in drawing 5 (b), and the ONO film 25 is formed in the whole surface and it is shown in drawing 5 (c), only the memory section 11 is covered by the resist 26, and the ONO film 25 of the circumference circuit section 18 is removed. However, it is SiO2 of the circumference circuit section 18 at this time. The film 23 is also removed. Then, as shown in drawing 5 (d), it is SiO2 as gate dielectric film to the front face of the component

active region of the circumference circuit section 16. After forming the film 23 again, the polycrystal Si film 27 is made to deposit on the whole surface, and Lynn is added.
[0008] Next, it is WSix as shown in drawing 5 (e). The silicide film of film 31 grade is made to deposit on the whole surface, and they are the polycrystal Si film 27 and WSix. The polycide film 32 is formed by the film 31. And a resist 33 is processed into the pattern of the control gate electrode 15 of the storage transistor 13, and the control gate electrode of the circumference circuit transistor 19.
[0009] Next, it is WSix where only the circumference circuit section 18 is covered by another resist (not shown), after having used the resist 33 as the mask, etching the polycide film 32 and the ONO film 25 continuously and exfoliating a resist 33, as shown in drawing 5 (f). Film 31 **** is used as a mask and the polycrystal Si film 24 of the memory section 11 is etched. And WSix Film 31 grade is used as a mask and it is N+ in the Si substrate 21. A diffusion layer 34 is formed and the storage transistor 13 and the circumference circuit transistor 19 are completed. Then, a well-known process is performed further conventionally.
[0010] With the storage transistor 13 of the memory section 11 in the 1st conventional example manufactured as mentioned above, the polycrystal Si film 24 is the floating-gate electrode 14, the ONO film 25 is an insulator layer for capacity coupling, and the polycide film 32 has become the control gate electrode 15. Moreover, with the circumference circuit transistor 19 of the circumference circuit section 18, the polycide film 32 is a control gate electrode.
[0011] Drawing 6 shows the memory sections 11, such as EPROM of eight steps of NAND molds, and a flash EEPROM. In eight steps of these NAND mold non-volatile semiconductor memories, eight storage transistors 13 share a diffusion layer 16 one by one, and are arranged at the serial, and one more selection transistor 35 is arranged at each serial at the both sides of eight storage transistors 13.
[0012] Although the floating-gate electrode 14 is also formed in each storage transistor 13 besides the control gate electrode 15 like the case of an above-mentioned NOR mold non-volatile semiconductor memory, only the control gate electrode 15 is formed in the selection transistor 35. The contact hole 17 for bit lines is formed on the diffusion layer 16 of an opposite hand in the storage transistor 13 of one selection transistor 35.
[0013] Drawing 7 shows the selection transistor 35 among the 2nd conventional examples of this invention which is the NAND mold non-volatile semiconductor memory shown in drawing 6 . SiO2 which is gate dielectric film with the storage transistor 13 of this 2nd conventional example The polycrystal Si film 36 on the film 23, and SiO2 The film 37 and the polycrystal Si film 38 are the insulator layer and the control gate electrode 15 the floating-gate electrode 14 and for capacity coupling, respectively.
[0014] For this reason, as shown in drawing 7 , the polycrystal Si film 38 is made into the shunt of the polycrystal Si film 36, and the polycrystal Si film 36 and 38 two-layer [ these ] constitutes the control gate electrode 15 from the selection transistor 35. That is, they are the polycrystal Si film 38 and SiO2 in the predetermined location of the memory section 11. The contact hole 41 was formed in the film 37, and the polycrystal Si film 36 and 38 comrades are electrically connected through the aluminum film 42 which covered and formed this contact hole 41.
[0015]
[Problem(s) to be Solved by the Invention] However, in the 1st conventional example shown in drawing 5 , compared with the level difference in the circumference circuit transistor 19, the level difference in the storage transistor 13 is large so that clearly also from drawing 5 (f). For this reason, the aspect ratio of the contact hole 17 is large, and it is unreliable. Moreover, since flattening is not easy, high integration by multilayer-interconnection-izing is also difficult. And since it is necessary to form the two-layer polycrystal Si film 24 and 27, compared with the usual insulated-gate field-effect transistor, there are many production processes and a manufacturing cost is high.
[0016] Moreover, in order to connect the polycrystal Si film 36 and 38 comrades electrically, the contact hole 41 and the aluminum film 42 are required of the 2nd conventional example

shown in drawing 7 . However, it is necessary to make a pitch larger than the polycrystal Si film 36 and 38, and to enlarge the dimension of the contact hole 41 by the aluminum film 42 patterning is not easy the film, compared with the polycrystal Si film 36 and 38, for the aluminum film 42 which is not good as for step coverage nature so that clearly also from drawing 7 (b). Therefore, it is difficult to reduce memory cell area and to attain high integration in this 2nd conventional example.

[0017]

[Means for Solving the Problem] The laminating gate mold non-volatile semiconductor memory of claim 1 The floating-gate electrode 14 is formed through the 1st insulator layer 23 on the channel field. The 1st insulated-gate field-effect transistor 13 by which the laminating of the 1st control gate electrode 15 is carried out through the 2nd insulator layer 25 and 37 on this floating-gate electrode 14, In the laminating gate mold non-volatile semiconductor memory which has the 2nd insulated-gate field-effect transistor 19 and 35 by which the 2nd control gate electrode 15 is formed on the channel field through the 3rd insulator layer 23 of the same layer as said 1st insulator layer 23 It is characterized by said 2nd control gate electrode 15 consisting of said 1st electric conduction film 24 and the 2nd electric conduction film 31 and 38 by which the laminating is carried out on 36 in the same layer as the 1st electric conduction film 24 and 36 of the same layer as said floating-gate electrode 14, and said 1st control gate electrode 15.

[0018] The laminating gate mold non-volatile semiconductor memory of claim 2 is characterized by said 1st control gate electrode 15 consisting of the semi-conductor film 38 in the laminating gate mold non-volatile semiconductor memory of claim 1.

[0019] The laminating gate mold non-volatile semiconductor memory of claim 3 is characterized by said 1st control gate electrode 15 consisting of the silicide film 31 in the laminating gate mold non-volatile semiconductor memory of claim 1.

[0020] The laminating gate mold non-volatile semiconductor memory of claim 4 is characterized by preparing the semi-conductor nitride in the pair plane of composition with said 1st control gate electrode 15 among said 2nd insulator layer 25 and 37 in the laminating gate mold non-volatile semiconductor memory of claims 2 or 3.

[0021]

[Function] In the laminating gate mold non-volatile semiconductor memory of claims 1-3, the floating-gate electrode 14 and the 1st control gate electrode 15 in the 1st insulated-gate field-effect transistor 13 consist of the electric conduction film 24 and 36 of the same layer, and 31 and 38 with the 1st [ which constitutes the 2nd control gate electrode 15 in the 2nd insulated-gate field-effect transistor 19 and 35 ], and 2nd electric conduction film 24 and 36, and 31 and 38, respectively.

[0022] For this reason, compared with the structure where any of the floating-gate electrode 14 or the 1st control gate electrode 15 they are consists of both 31 and 38 [ the 1st and 2nd electric conduction film 24 and 36 and ], the level difference in the 1st insulated-gate field-effect transistor 13 is small, flattening is easy, moreover it is not necessary to use the 1st and the 2nd electric conduction film 24, 36, and 31, and electric conduction film 42 other than 38, and a production process is simple.

[0023] Moreover, in the 2nd insulated-gate field-effect transistor 19 and 35, the 2nd control gate electrode 15 is constituted by the 1st electric conduction film 24 and 36, this 1st electric conduction film 24, and the 2nd electric conduction film 31 and 38 by which the laminating is carried out on 36, and the insulator layer does not intervene between 31 and 38 [ these / 1st /, the 2nd electric conduction film 24 and 36, and ]. For this reason, the contact hole 41 for connecting electrically the 1st and the 2nd electric conduction film 24, 36, and 31, and 38 comrades and the additional electric conduction film 42 are unnecessary, and these are able to reduce memory cell area compared with required structure.

[0024] In case the natural oxidation film is removed from the front face of the 1st electric conduction film 24 and 36 which constitutes the 2nd control gate electrode 19 and 35 from a laminating gate mold non-volatile semiconductor memory of claim 4, it is possible to prevent that the 2nd insulator layer 25 and 37 in the 1st insulated-gate field-effect transistor 13 is

etched by the semi-conductor nitride.
[0025] Moreover, even if the 1st control gate electrode 15 consists of the silicide film 31, the adhesion of the 1st control gate electrode 15 and the 2nd insulator layer 25 is good because of a semi-conductor nitride, and it can prevent that the constituent of the 1st control gate electrode 15 invades into the 2nd insulator layer 25, and the membraneous quality of the 2nd insulator layer 25 deteriorates by the semi-conductor nitride.
[0026]
[Example] Hereafter, the 1st and 2nd examples of this invention are explained, referring to drawing 1 -3. In addition, the same sign is given to drawing 5 , the 1st and 2nd conventional example shown in 7, and the corresponding component.
[0027] Drawing 1 shows the approach for manufacturing the 1st example of this invention which is the NOR mold non-volatile semiconductor memory shown in drawing 4 about the storage transistor 13 of the memory section 11, and the circumference circuit transistor 19 of the circumference circuit section 18. The same process is substantially performed with the case where the 1st conventional example shown in drawing 5 is manufactured until it adds Lynn on the polycrystal Si film 24 made to deposit on the whole surface also by this manufacture approach, as shown in drawing 1 (a).
[0028] However, it leaves the polycrystal Si film 24 also all over the circumference circuit section 18 at the same time it leaves the polycrystal Si film 24 of the shape of stripes which extends in the direction vertical to the extension direction of the control gate electrode 15 formed behind at RIE to the polycrystal Si film 24 after that to the memory section 11, in order to manufacture this 1st example.
[0029] Next, as shown in drawing 1 (b), the ONO film 25 is formed in the front face of polycrystal Si film 24 grade, further, as shown in drawing 1 (c), only the memory section 11 is covered by the resist 26, and the ONO film 25 of the circumference circuit section 18 is removed by plasma etching etc.
[0030] Next, as shown in drawing 1 (d), after exfoliating a resist 26, the natural oxidation film on the polycrystal Si film 24 in the circumference circuit section 18 (not shown) is etched with fluoric acid water. SiO2 by the side of the upper layer of the ONO film [ in / at this time / the memory section 11 ] 25 Since the film is also etched simultaneously, it is expected, and it is this SiO2. Membranous thickness is thickened.
[0031] Then, WSix The silicide film of film 31 grade is made to deposit on the whole surface, it sets only in the circumference circuit section 18, and they are the polycrystal Si film 24 and WSix. The polycide film 43 is formed by the film 31. And a resist 33 is processed into the pattern of the control gate electrode 15 of the storage transistor 13, and the control gate electrode of the circumference circuit transistor 19.
[0032] Next, as shown in drawing 1 (e), a resist 33 is used as a mask, and it is WSix. Only the film 31 is etched by RIE. Then, by the high selection-ratio oxide film etching system, as shown in drawing 1 (f), the ONO film 25 of the memory section 11 is etched, and the polycrystal Si film 24 of the memory section 11 and the circumference circuit section 18 is etched succeedingly. And WSix Film 31 grade is used as a mask and it is N+ in the Si substrate 21. A diffusion layer 34 is formed and the storage transistor 13 and the circumference circuit transistor 19 are completed. Then, a well-known process is performed further conventionally.
[0033] With the storage transistor 13 of the memory section 11 in the 1st example manufactured as mentioned above, the polycrystal Si film 24 is the floating-gate electrode 14, the ONO film 25 is an insulator layer for capacity coupling, and it is WSix. The film 31 is the control gate electrode 15. Moreover, with the circumference circuit transistor 19 of the circumference circuit section 18, the polycide film 43 is a control gate electrode.
[0034] And a level difference [ in / so that clearly from drawing 1 (f) / the storage transistor 13 ] is the polycrystal Si film 24 and WSix which it is only large about 20nm compared with the level difference in the circumference circuit transistor 19 because of the ONO film 25, and are the floating-gate electrode 14 and the control gate electrode 15 of the storage transistor 13. The level difference by the film 31 and the level difference by the polycide film 43 which is the control gate electrode of the circumference circuit transistor 19 do not

almost have a difference.

[0035] Moreover, while processes, such as deposition of the polycrystal Si film 27 and addition of Lynn, are unnecessary since the polycrystal Si film 27 is not used in this 1st example if the 1st conventional example shown in drawing 5 is compared with this 1st example, in case the polycrystal Si film 24 is etched, processes, such as patterning of a wrap resist, are also unnecessary in the circumference circuit section 18, and this 1st example of a production process is simpler.

[0036] In addition, at the 1st example, it is the polycrystal Si film 24 and WSix of the memory section 11. Although the ONO film 25 is used as an insulator layer for capacity coupling between film 31, the ONON film which prepared the SiN film on this ONO film 25 may be used as an insulator layer for capacity coupling. If this ONON film is used, they are the ONO film 25 and WSix. Adhesion with the film 31 is good, and WSix. W in the film 31, Si, etc. are SiO2 by the side of the upper layer of the ONO film 25. It can prevent that invade into the film and the membraneous quality of the ONO film 25 deteriorates.

[0037] Moreover, SiO2 by the side of the upper layer of the ONO film 25 in the memory section 11 if this ONON film is used, in case the natural oxidation film on the polycrystal Si film 24 in the circumference circuit section 18 will be etched with fluoric acid water by the process of drawing 1 (d) Since the film can also prevent being etched simultaneously, it is expected, and it is this SiO2. It becomes unnecessary to thicken membranous thickness.

[0038] Drawing 2 and 3 show the approach for manufacturing the 2nd example of this invention which is the NAND mold non-volatile semiconductor memory shown in drawing 6 about the storage transistor 13 of the memory section 11, and the selection transistor 35. Also with this manufacture approach, it is SiO2 as gate dielectric film to the front face of a component active region. The same process is substantially performed with the case where the 1st conventional example shown in drawing 5 is manufactured until it forms the film 23.

[0039] As shown in drawing 2 (a) after that, the polycrystal Si film 36 is made to deposit on the whole surface with a CVD method, and in order to manufacture this 2nd example, as shown in drawing 2 (b), a resist 44 is processed into a wrap pattern for the field which should form the part and the selection transistor 35 of the shape of stripes which specifies the width of face of the floating-gate electrode 14 of the storage transistor 13 which should be arranged to a serial on the polycrystal Si film 36. And this resist 44 is used as a mask and RIE to the polycrystal Si film 36 is performed.

[0040] Next, as shown in drawing 2 (c), after exfoliating a resist 44, the polycrystal Si film 36 is oxidized, and it is SiO2 to the front face. The film 37 is formed. Then, SiO2 of the field which should cover only the field which should form the storage transistor 13 by the resist 45, and should form the selection transistor 35 as shown in drawing 2 (d) The film 37 is etched. And as shown in drawing 2 (e), after exfoliating a resist 45, the polycrystal Si film 38 is made to deposit on the whole surface with a CVD method.

[0041] Next, as shown in drawing 3 (a), a resist 46 is processed into the pattern of the control gate electrode 15 of the storage transistor 13 and the selection transistor 35 on the polycrystal Si film 38, this resist 46 is used as a mask, and RIE to the polycrystal Si film 38 is performed. And SiO2 which used the resist 46 as the mask succeedingly and has been exposed from this resist 46 as shown in drawing 3 (b) RIE to the film 37 is performed.

[0042] Next, as shown in drawing 3 (c), a resist 46 is used as a mask further succeedingly, and RIE to the polycrystal Si film 36 exposed from this resist 46 is performed. And after exfoliating a resist 46, polycrystal Si film 38 grade is used as a mask, a diffusion layer 16 is formed into the Si substrate 21, and the storage transistor 13 and the selection transistor 35 are completed. Then, a well-known process is performed further conventionally.

[0043] With the storage transistor 13 of the 2nd example manufactured as mentioned above, the polycrystal Si film 36 and 38 is the floating-gate electrode 14 and the control gate electrode 15, respectively so that clearly also from drawing 3 (c), and it is SiO2. It is an insulator layer for the film 37 to carry out capacity coupling of these polycrystal Si film 36 and the 38 comrades. However, at the selection transistor 35, it is SiO2. The film 37 does not exist but the top face of the polycrystal Si film 36 and the underside of the polycrystal Si film

38 which are both the control gate electrodes 15 are extensively in contact.

[0044] Therefore, these are able not to need the contact hole 41 and the aluminum film 42 for connecting the polycrystal Si film 36 and 38 comrades electrically for the appearance of the 2nd conventional example shown in drawing 7 , but to reduce memory cell area to it in this 2nd example, compared with the required 2nd conventional example.

[0045] In addition, it is SIO2 as an insulator layer for carrying out capacity coupling of the polycrystal Si film 36 and 38 comrades which are the floating-gate electrode 14 and the control gate electrode 15 of the storage transistor 13 in this 2nd example. Although the film 37 is used, it is this SiO2. The SiN film may be prepared on the film 37 and the ONO film 25, the ONON film, etc. may be used like the 1st above-mentioned example.

[0046]

[Effect of the Invention] Since the level difference [ in / with the laminating gate mold non-volatile semiconductor memory of claims 1-3 / the 1st insulated-gate field-effect transistor ] is small, the aspect ratio of a contact hole is small and it is reliable, and since flattening is easy, high integration by multilayer-interconnection-izing is also possible. And since a manufacturing cost is low since the production process is simple, and it is possible to reduce memory cell area, the further high integration is possible.

[0047] It is possible to prevent that the 2nd insulator layer in the 1st insulated-gate field-effect transistor is etched in the laminating gate mold non-volatile semiconductor memory of claim 4, the adhesion of the 1st control gate electrode and the 2nd insulator layer is good, and since it can prevent that the constituent of the 1st control gate electrode invades into the 2nd insulator layer, and the membraneous quality of the 2nd insulator layer deteriorates, dependability and a data-hold property are high.

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[Translation done.]

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional side elevation showing the manufacture approach of the 1st example of this invention in order of a process.
[Drawing 2] The first half of the manufacture approach of the 2nd example of this invention is shown in order of the process, and it is a sectional side elevation in the location which meets the S-S line of drawing 6 .
[Drawing 3] The second half of the manufacture approach of the 2nd example is shown in order of the process, and it is a sectional side elevation in the location which meets the S-S line of drawing 6 .
[Drawing 4] It is the top view of the memory section in the laminating gate mold non-volatile semiconductor memory of the NOR mold which can apply this invention.
[Drawing 5] It is the sectional side elevation showing the manufacture approach of the 1st conventional example of this invention in order of a process.
[Drawing 6] It is the top view of the memory section in the laminating gate mold non-volatile semiconductor memory of the NAND mold which can apply this invention.
[Drawing 7] The important section of the 2nd conventional example of this invention is shown, (a) is a sectional side elevation and (b) is a top view.
[Description of Notations]
13 Storage Translator
14 Floating-Gate Electrode
15 Control Gate Electrode
19 Circumference Circuit Transistor
23 SiO2 Film
24 Polycrystal Si Film
25 ONO Film
31 WSix Film
35 Selection Transistor
36 Polycrystal Si Film
37 SiO2 Film
38 Polycrystal Si Film

[Translation done.]